

Drafts  
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```
((single near3 event near3 upset) SEU) near3 (resist$3 imped$3))  
(53) (((single near3 event near3 upset) SEU) near3 (resist$3 imped$3))) an  
(33) (((single near3 event near3 upset) SEU) near3 (resist$3 imped$3))) a  
(0) (((single near3 event near3 upset) SEU) near3 (resist$3 imped$3))) a  
(73) (((single near3 event near3 upset) SEU) near5 (resist$3 imped$3))  
(12) (((single near3 event near3 upset) SEU) near5 (resist$3 imped$3))) an  
(0) (((single near3 event near3 upset) SEU) near5 (resist$3 imped$3))) and  
(0) (((single near3 event near3 upset) SEU) near5 (resist$3 imped$3))) and  
(0) (((single near3 event near3 upset) SEU) near5 (resist$3 imped$3))) and  
(48914) resist$3 near2 transistor  
(76238) transistor near3 resistor  
(59077) (control$5 program$5 adjust$4 variable) with transistor with (resis  
(18985) (control$5 program$5 adjust$4 variable) near4 transistor near4 (res  
(838) (single near3 event near3 upset) or SEU  
(841) ((single near3 event near3 upset) SEU)  
(143) (((single near3 event near3 upset) SEU)) and memory and (resist$3)  
(21) (US-6369630-S or US-6271568-S or US-6180984-S or US-6058041-S or US-53  
(7) ((US-6369630-S or US-6271568-S or US-6180984-S or US-6058041-S or US-53  
(0) 10/125,666  
(6400) resist$3 adj transistor
```

Favorites

DB: USPAT:US POPUL:EPD:PO:DERWENT:BM:TOP

Default operator: OP

Date:

Highlight all hit terms only

	Type	L #	Hits	Search Text	DB:	Time Stamp	Cc
1	BRS	L1	6	(((single near3 event near3 upset) SEU) near5 (resist\$3 imped\$3))) and (resist\$3 adj transistor)	USPAT	2004/05/24 15:36	
2	BRS	L2	19	(((single near3 event near3 upset) SEU) near5 (resist\$3 imped\$3))) and (transistor near3 resistor)	USPAT	2004/05/24 15:37	
3	BRS	L3	30	((single near3 event near3 upset) SEU) and ((var\$5 program\$5 adjust\$4) near3 (impedance resistance))	USPAT	2004/05/24 15:37	
4	BRS	L4	59	(((single near3 event near3 upset) SEU)) and ohm	USPAT	2004/05/24 15:37	
5	BRS	L5	48	((single near3 event near3 upset) or SEU) and ((resist\$4 imped\$5) near2 value)	USPAT	2004/05/24 15:37	
6	BRS	L6	24	((control\$5 program\$5 adjust\$4 variable) with transistor with (resist\$4 imped\$4)) and ((single near3 event near3 upset) or SEU)	USPAT	2004/05/24 15:37	

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